*Figure 1*

Moore's Law Vs Bandwidth Demand

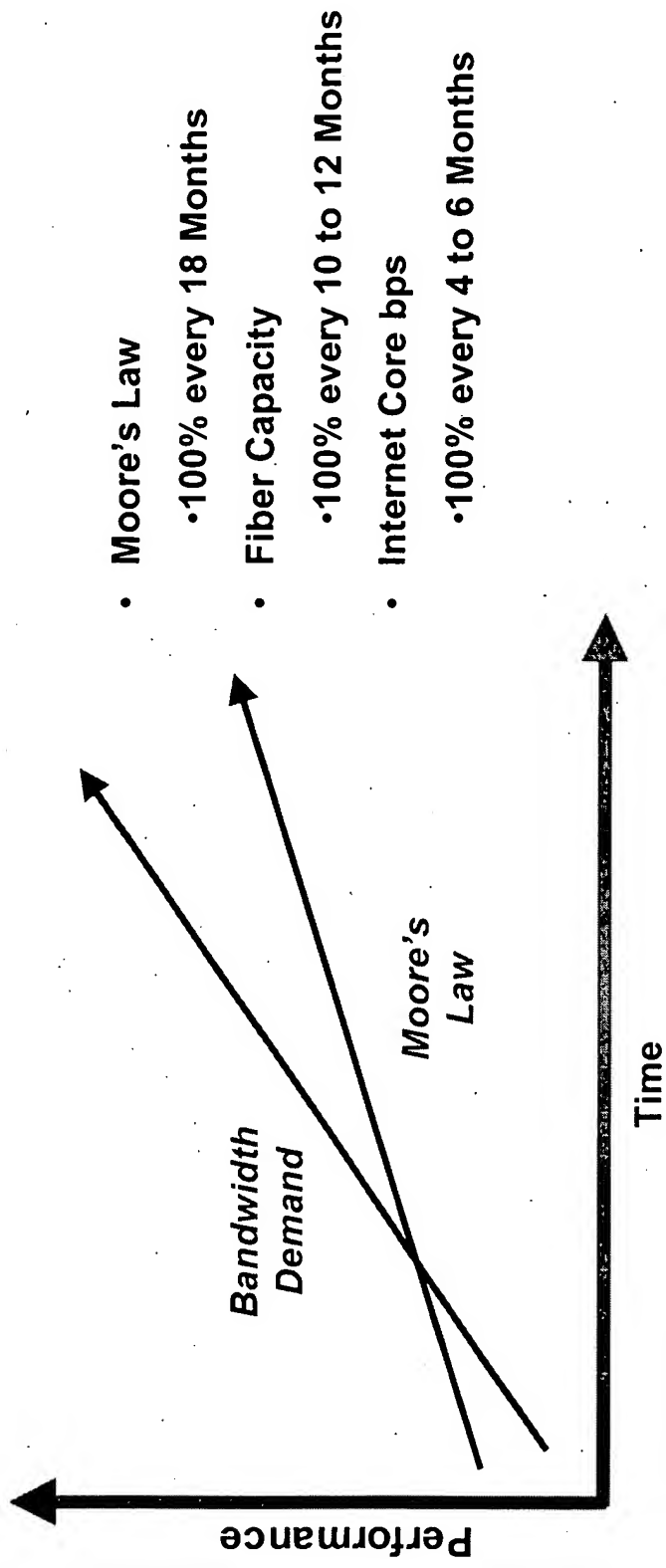
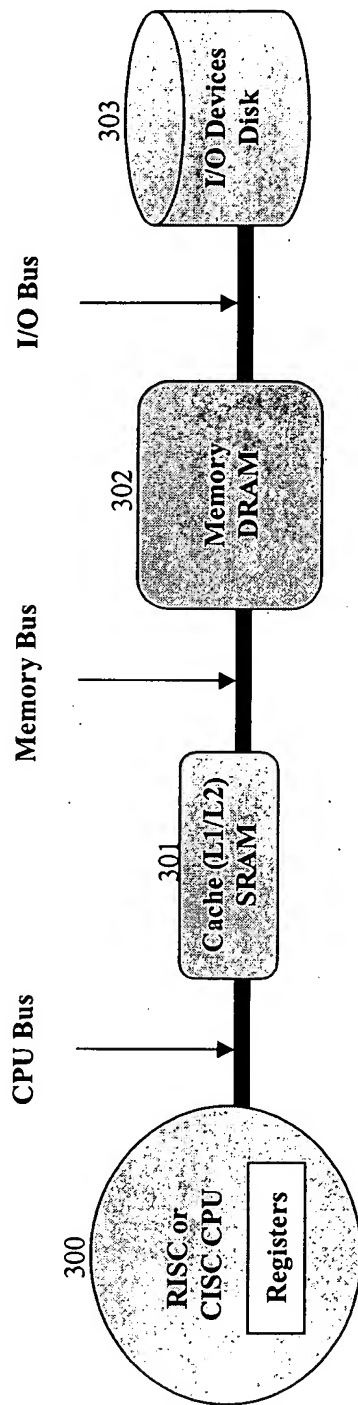


Figure 2

Memory Hierarchy in a Computer System



| | |
|------------------|------------------|
| Registers: | Disk Storage: |
| 100 to 500 Bytes | 4G - 256G Bytes |
| @200 MHz = 5 nS | @200 MHz = 10 nS |

| | |
|------------------|------------------|
| Cache: | Main Memory: |
| 32K - 512K Bytes | 32M - 4G Bytes |
| @200 MHz = 10 nS | @200 MHz = 10 nS |

Figure 3

Memory Management Subsystems

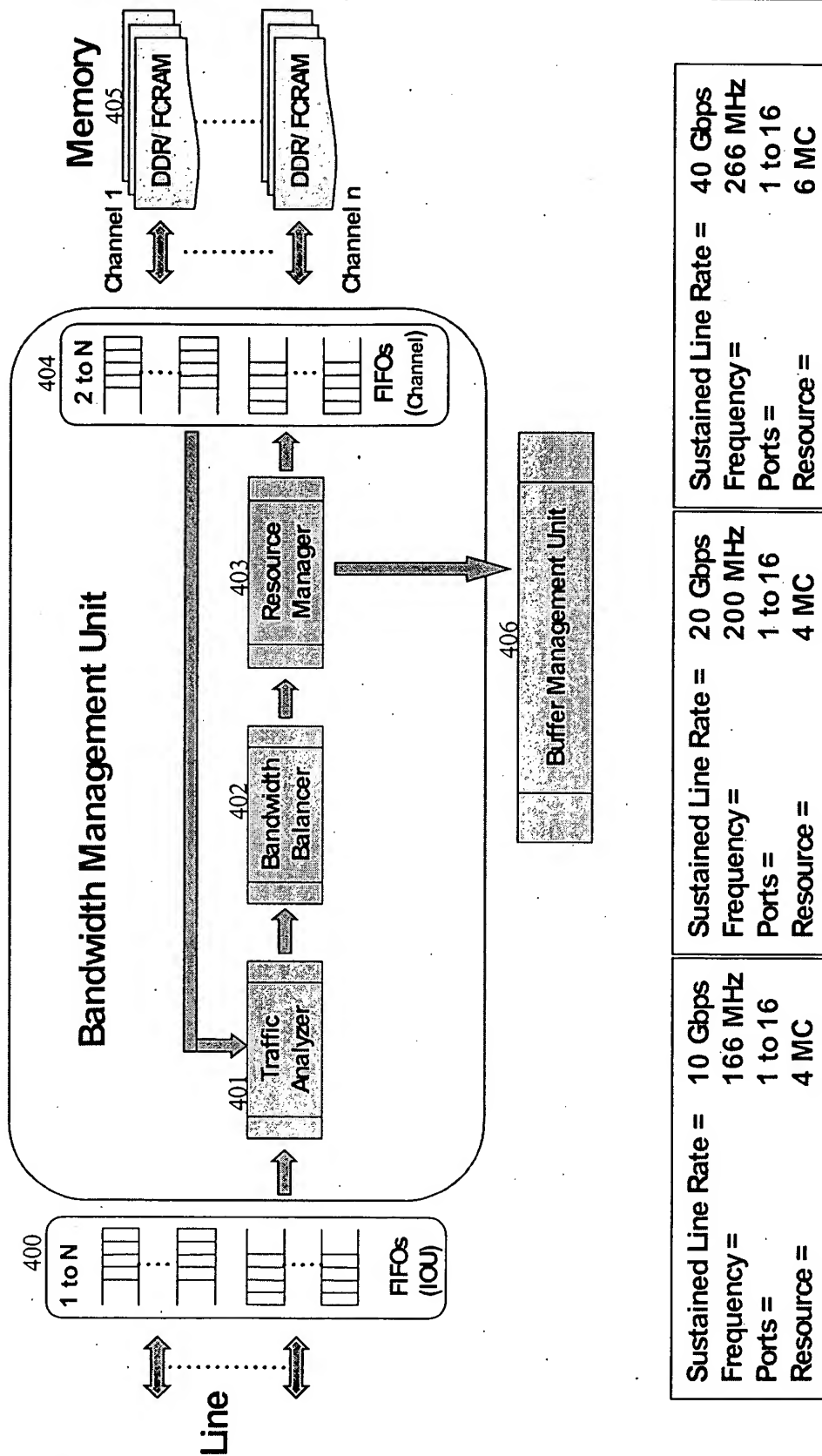


Figure 4

Bandwidth Balancer Data Structure

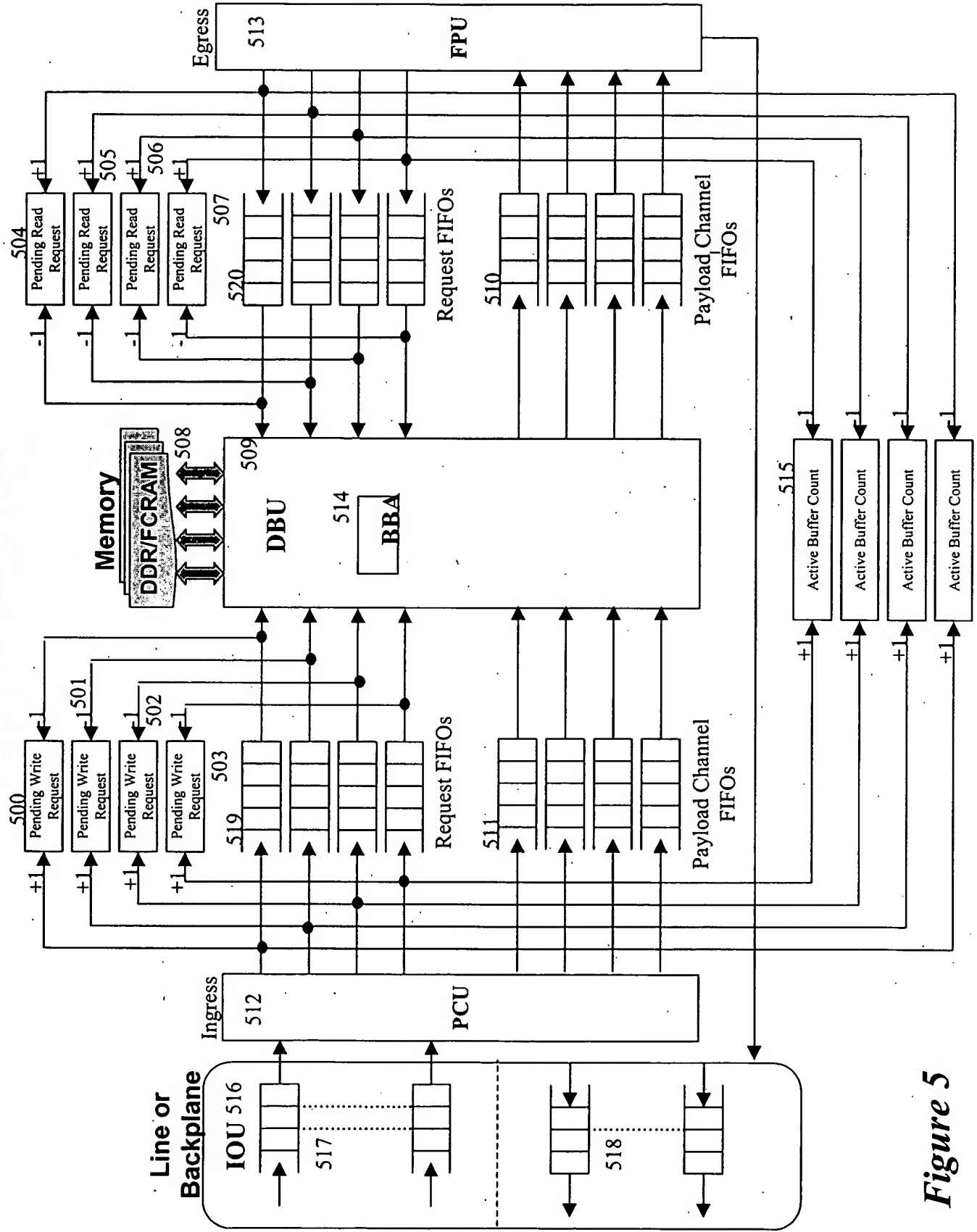


Figure 5

Payload Channel Sequence Table Structure

| Val | EoP | 1 st Buffer Location | Val | EoP | 2 nd Buffer Location | Val | EoP | 3 rd Buffer Location | Val | EoP | 4 th Buffer Location |
|-----|-----|---------------------------------|-----|-----|---------------------------------|-----|-----|---------------------------------|-----|-----|---------------------------------|
| 0 | 0 | 10 | 1 | 1 | 00 | 1 | 1 | 01 | 1 | 1 | 01 |
| 1 | 1 | 01 | 1 | 0 | 11 | 1 | 0 | 00 | 0 | 0 | 00 |
| 1 | 0 | 00 | 1 | 0 | 01 | 1 | 1 | 10 | 1 | 1 | 10 |

601

Line Pointer 1

602

Line Pointer 2

603

Line Pointer 3

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

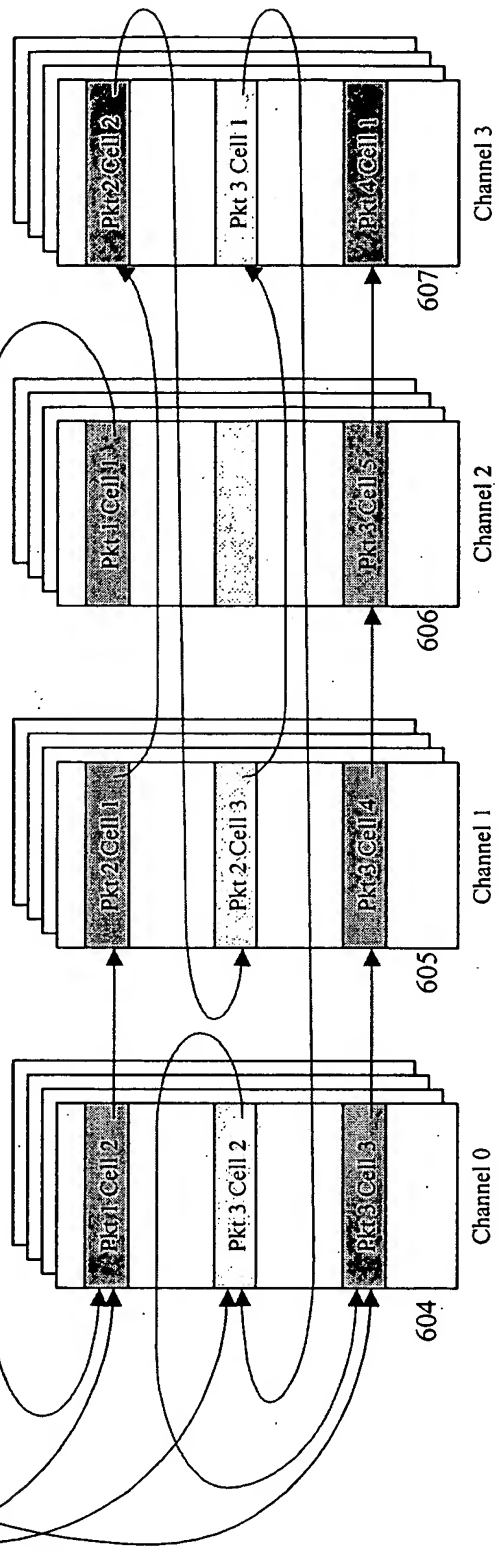


Figure 6

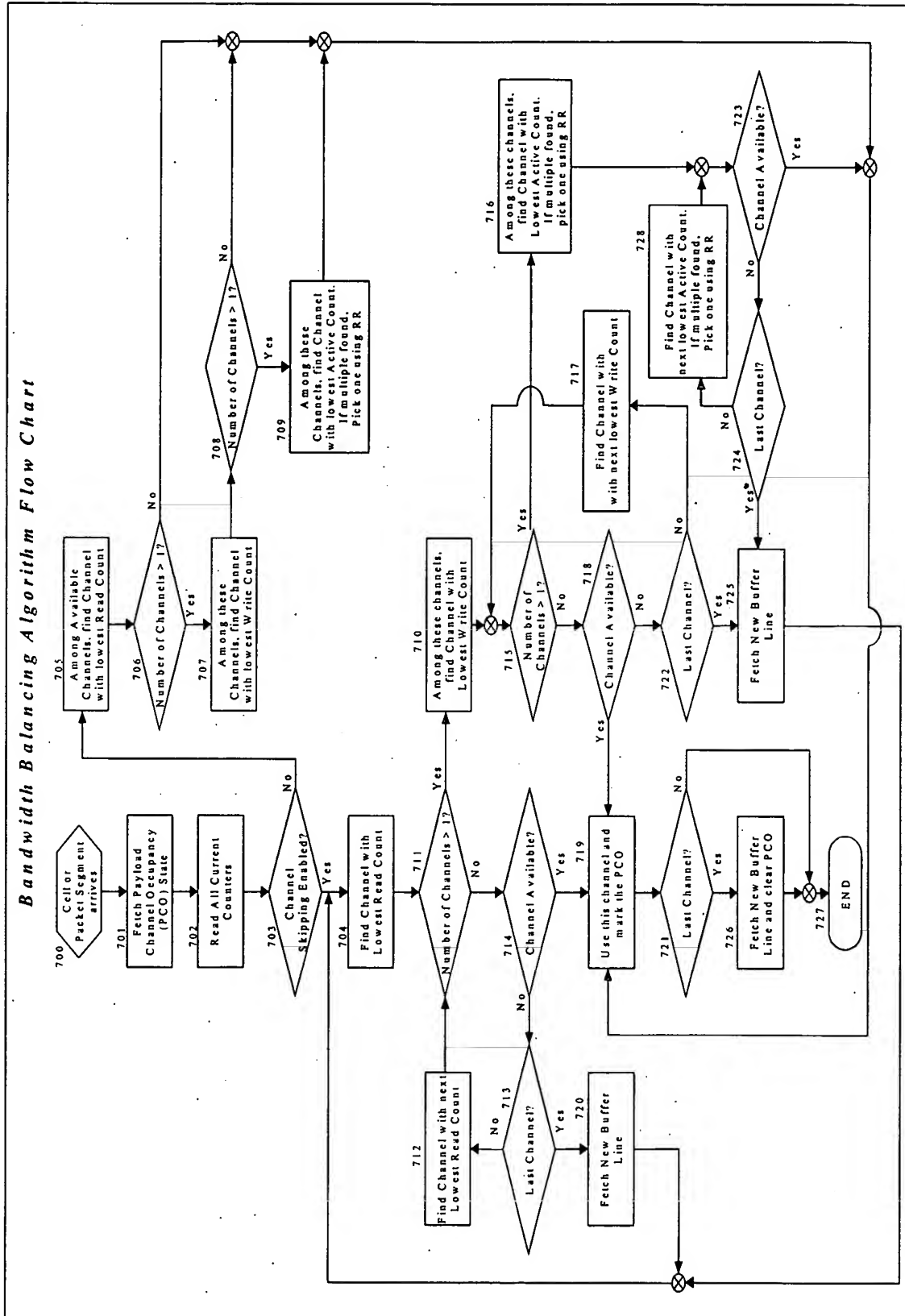


Figure 7